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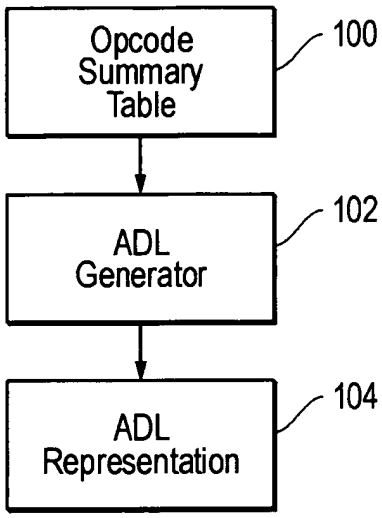

FIG. 1

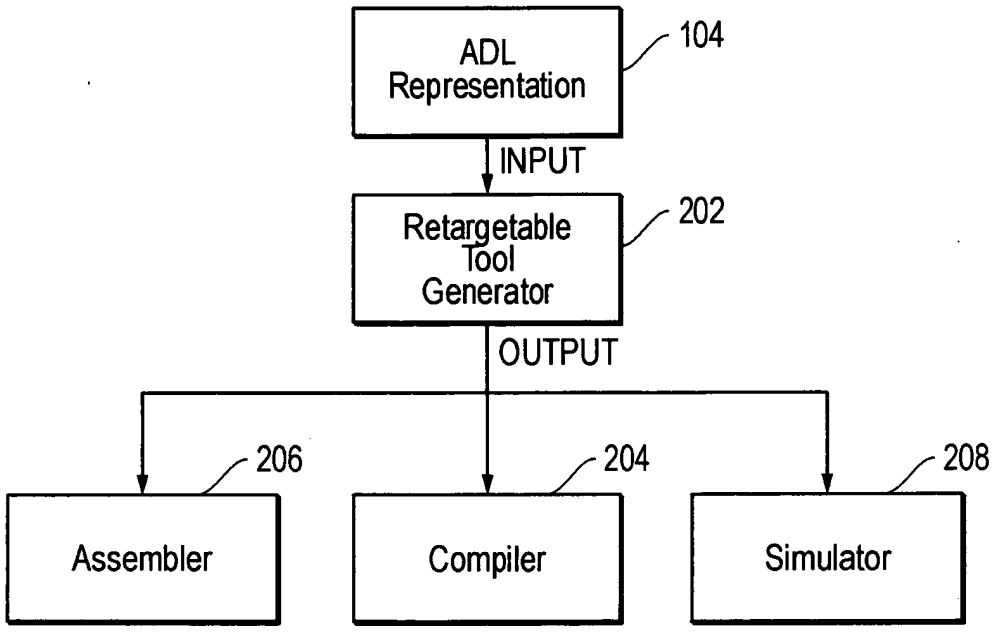

FIG. 2

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700

Arm Instruction Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Instruction	Description	Opnd Order
cond				0	0	1	*	*	*	*	S		Rn				Rd			rotate_imme				8_bit_immediate								*Data_proc_imm*	*Data_proc_imm*	cond
cond				0	0	1	1	0	1	0	S	0	0	0	0		Rd			rotate_imme				8_bit_immediate								MOVI		S
cond				0	0	1	1	1	1	1	S	0	0	0	0		Rd			rotate_imme				8_bit_immediate								MVNI		cp_num
cond				0	0	1	0	1	0	0	S		Rn				Rd			rotate_imme				8_bit_immediate								ADDI		CRd
cond				0	0	1	0	1	0	1	S		Rn				Rd			rotate_imme				8_bit_immediate								ADCI		opcode_1 CDP
cond				0	0	1	0	1	1	0	S		Rn				Rd			rotate_imme				8_bit_immediate								SUBI		opcode_1
cond				0	0	1	0	1	1	1	S		Rn				Rd			rotate_imme				8_bit_immediate								SBCI		Rd
cond				0	0	1	1	0	0	1	S		Rn				Rd			rotate_imme				8_bit_immediate								RSBI		CRn
cond				0	0	1	1	0	1	0	S		Rn				Rd			rotate_imme				8_bit_immediate								RSCI		CRm
cond				0	0	1	1	0	1	1	S		Rn				Rd			rotate_imme				8_bit_immediate								ANDI		opcode_2
cond				0	0	1	1	1	0	0	S		Rn				Rd			rotate_imme				8_bit_immediate								EORI		Rn
cond				0	0	1	1	1	0	1	S		Rn				Rd			rotate_imme				8_bit_immediate								ORRI		12_bit_offset
cond				0	0	1	1	1	1	0	S		Rn				Rd			rotate_imme				8_bit_immediate								BICI		8-bit_offset
cond				0	0	1	1	1	1	1	S		Rn				Rd			rotate_imme				8_bit_immediate								CMPI		8_bit_immediate
cond				0	0	1	1	0	1	0	S		Rn			0	0	0	0	rotate_imme				8_bit_immediate								CMNI		rotate_Immed
cond				0	0	1	1	0	1	1	S		Rn			0	0	0	0	rotate_imme				8_bit_immediate								TSTI		RdLo
cond				0	0	1	1	0	0	0	S		Rn			0	0	0	0	rotate_imme				8_bit_immediate								TEQI		RdHi
cond				0	0	1	1	0	0	1	S		Rn			0	0	0	0	rotate_imme				8_bit_immediate								*Data_proc_imm*	*Data Processing*	Rm
cond				0	0	0	*	*	*	*	S		Rn				Rd			shift_immed				shift	0		Rm					*Data_proc_imm*		shift
cond				0	0	0	1	1	0	1	S	0	0	0	0		Rd			shift_immed				shift	0		Rm					MOVS		shift_Immed
cond				0	0	0	1	1	1	1	S	0	0	0	0		Rd			shift_immed				shift	0		Rm					MVNS		Rs
cond				0	0	0	0	1	0	0	S		Rn				Rd			shift_immed				shift	0		Rm					ADDS		register_list
cond				0	0	0	0	1	0	1	S		Rn				Rd			shift_immed				shift	0		Rm					ADCS		register_list_15
cond				0	0	0	0	1	1	0	S		Rn				Rd			shift_immed				shift	0		Rm					SUBS		24_bit_immedia
cond				0	0	0	0	1	1	1	S		Rn				Rd			shift_immed				shift	0		Rm					SBCS		
cond				0	0	0	0	0	1	1	S		Rn				Rd			shift_immed				shift	0		Rm					RSBS		
cond				0	0	0	0	0	1	0	S		Rn				Rd			shift_immed				shift	0		Rm					RSCS		
cond				0	0	0	0	0	0	1	S		Rn				Rd			shift_immed				shift	0		Rm					ANDS		
cond				0	0	0	0	0	0	0	S		Rn				Rd			shift_immed				shift	0		Rm					EORS		
cond				0	0	0	0	0	0	1	S		Rn				Rd			shift_immed				shift	0		Rm					ORRS		
cond				0	0	0	1	1	1	0	S		Rn				Rd			shift_immed				shift	0		Rm					BICS		
cond				0	0	0	1	0	1	0	S		Rn			0	0	0	0	shift_immed				shift	0		Rm					CMPS		
cond				0	0	0	1	0	1	1	S		Rn			0	0	0	0	shift_immed				shift	0		Rm					CMNS		
cond				0	0	0	1	0	0	0	S		Rn			0	0	0	0	shift_immed				shift	0		Rm					TSTS		
cond				0	0	0	1	0	0	1	S		Rn			0	0	0	0	shift_immed				shift	0		Rm					TEQS		
cond				0	0	0	*	*	*	*	S		Rn				Rd			Rs		0		shift	1		Rm					*Data_proc_reg*	*Data_proc_register_shift*	
cond				0	0	0	1	1	0	1	S	0	0	0	0		Rd			Rs		0		shift	1		Rm					MOVR		
cond				0	0	0	1	1	1	1	S	0	0	0	0		Rd			Rs		0		shift	1		Rm					MVNR		
cond				0	0	0	0	1	0	0	S		Rn				Rd			Rs		0		shift	1		Rm					ADDR		
cond				0	0	0	0	1	0	1	S		Rn				Rd			Rs		0		shift	1		Rm					ADCR		
cond				0	0	0	0	0	1	0	S		Rn				Rd			Rs		0		shift	1		Rm					SUBR		
cond				0	0	0	0	0	1	1	S		Rn				Rd			Rs		0		shift	1		Rm					SBCR		
cond				0	0	0	0	0	0	1	S		Rn				Rd			Rs		0		shift	1		Rm					RSBR		
cond				0	0	0	0	0	0	0	S		Rn				Rd			Rs		0		shift	1		Rm					RSCR		
cond				0	0	0	0	0	0	1	S		Rn				Rd			Rs		0		shift	1		Rm					ANDR		
cond				0	0	0	0	0	0	0	S		Rn				Rd			Rs		0		shift	1		Rm					EORR		
cond				0	0	0	1	1	1	0	S		Rn				Rd			Rs		0		shift	1		Rm					ORRR		
cond				0	0	0	1	1	0	0	S		Rn				Rd			Rs		0		shift	1		Rm					BICR		
cond				0	0	0	1	0	1	0	S		Rn			0	0	0	0	Rs		0		shift	1		Rm					CMPR		
cond				0	0	0	1	0	1	1	S		Rn			0	0	0	0	Rs		0		shift	1		Rm					CMNR		
cond				0	0	0	1	0	0	0	S		Rn			0	0	0	0	Rs		0		shift	1		Rm					TSTR		
cond				0	0	0	1	0	0	1	S		Rn			0	0	0	0	Rs		0		shift	1		Rm					TEQR		
cond				0	0	0	0	0	0	*	S		Rd				Rn			Rs		1	0	0	1		Rm					*Multiply*	*Multiply*	
cond				0	0	0	0	0	0	0	S		Rd			0	0	0	0	Rs		1	0	0	1		Rm					MUL	Multiply	
cond				0	0	0	0	0	0	1	S		Rd				Rn			Rs		1	0	0	1		Rm					MLA	Multiply Accumulate	
cond				0	0	0	0	1	*	*	S		RdHi				RdLo			Rs		1	0	0	1		Rm					*Multiply Long*	*Multiply Long*	
cond				0	0	0	0	1	1	1	S		RdHi				RdLo			Rs		1	0	0	1		Rm					SMLAL	Signed Multiply Accumulate Long	
cond				0	0	0	0	1	1	0	S		RdHi				RdLo			Rs		1	0	0	1		Rm					SMULL	Signed Multiply Long	
cond				0	0	0	0	1	0	1	S		RdHi				RdLo			Rs		1	0	0	1		Rm					UMLAL	Unsigned Multiply Accumulate Lo	
cond				0	0	0	0	1	0	0	S		RdHi				RdLo			Rs		1	0	0	1		Rm					UMULL	Unsigned Multiply Long	
cond				0	0	0	1	0	R	0	0	1	1	1	1		Rd			0	0	0	0	0	0	0	0	0	0	0	0	MRS	Move from Status register	
cond				0	0	1	1	0	R	1	0	field_mask				1	1	1	1	rotate_immed				8_bit_immediate								MSRI	Move immediate to Status registe	
cond				0	0	0	1	0	R	1	0	field_mask				1	1	1	1	0	0	0	0	0	0	0	0	Rm				MSR	Move register to Status register	
cond				1	0	1	L	24_bit_signed_offset																								B(L)	Brach Instructio	Rd
cond				0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	Rm			BX	Brach and exch	Rm
cond				0	1	0	*	*	*	*	*	Rn				Rd				12_bit_offset												*Load/Store Imm*	*Load/Store Imm*	Rs
cond				0	1	0	P	U	0	W	1	Rn				Rd				12_bit_offset												LDRI		Rn
cond				0	1	0	P	U	1	W	1	Rn				Rd				12_bit_offset												LDRBI		
cond				0	1	0	0	U	1	1	1	Rn				Rd				12_bit_offset												LDRBTI		
cond				0	1	0	0	U	0	1	1	Rn				Rd				12_bit_offset												LDRTI		
cond				0	1	0	P	U	0	W	0	Rn				Rd				12_bit_offset												STRI		
cond				0	1	0	P	U	1	W	0	Rn				Rd				12_bit_offset												STRBI		
cond				0	1	0	0	U	1	1	0	Rn				Rd				12_bit_offset												STRBTI		

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FIG. 7

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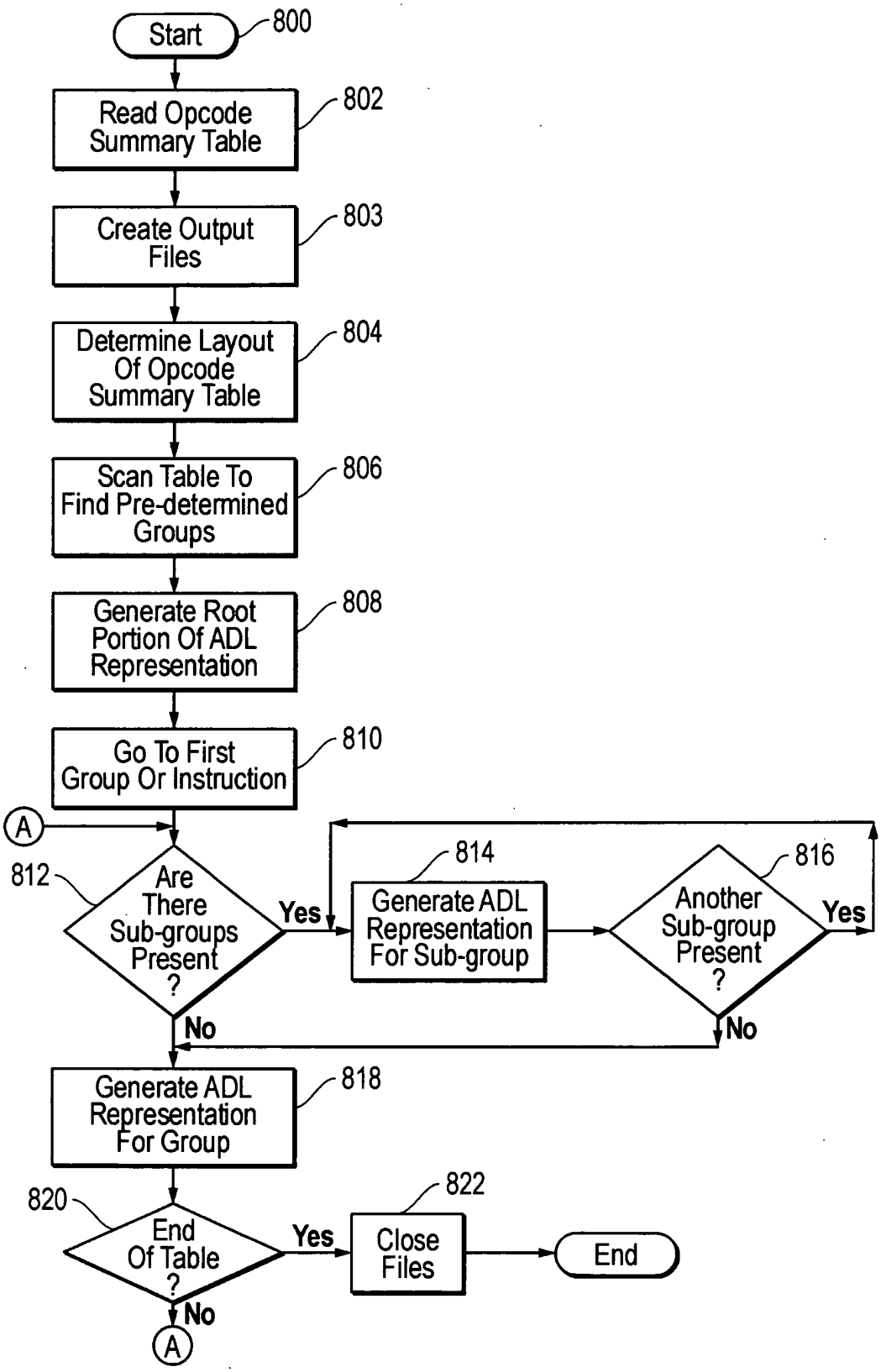

FIG. 8